CHAPTER 15

ELECTRONIC SCIENCE

Doctoral Theses

01. AGRAWAL (Niti)

Investigation and Mitigation of Partial Shading Mismatch Losses in Solar Photovoltaic Arrays.

Supervisors: Prof. Mridula Gupta and Prof. Avinashi Kapoor Th 27112

Abstract

This research aimed at increasing the fault tolerance of the PV array due to partial shading to enhance its output performance under partial shading conditions, without increasing the cost burden on PV system. Partial shading is one of major challenge faced by the field installed PV array as it can drastically reduce the output power of PV array. The output power losses (%) are much greater than the (%) shaded area of the array. PS leads to the appearance of multiple peaks in the powervoltage characteristics and even hot spots, which shorten the life span of modules. Partial shading extenuates the efficiency and reliability of PV system. Hence it is a major concern not only for PV system designers as well as for end consumers who expect a utility grade reliability of PV system. Mitigation of partial shading has attracted the attention of many researchers and different configurations of PV arrays have been proposed and examined over the years in this regard. These previous studies considered different configurations at the module level modules have been interconnected in different fashions within the array. Moreover, most of the studies have been conducted in simulated environment. Interconnecting modules in TCT or BL scheme, or reconfiguring TCT using mathematical puzzles thought have shown power enhancement of the array under PSC but increases complexity, requires long installation wires which can increase the wire losses and additional electrical/ electronic equipment which increases the cost of the PV system, especially when exerted over large PV array. This can reduce the practical significance of these configurations as the PV industry constantly strive to increase the power output and reduce cost at the same time.

Contents

1. Introduction 2. Instrumentation and procedures. Fault tolerance due to shading in photovoltaic modules with different interconnected solar cell networks. 4. Novel hybrid TCT-S PV array configuration. 5. Comparative energy yield of TCT-S and S-S KPV array under uniform irradiance and partial shading conditions. 6. Conclusion and scope of the future work. Reprints of the published papers.

02. GAHLOT (Ajay Pratap Singh)

Study of Nanostructured Based Design of Devices for Gas Sensing Application. Supervisors: Prof. Mridula Gupta and Prof. Avinashi Kapoor Th 27113

Abstract

Zinc oxide (ZnO) is a semiconducting piezoelectric, and optical waveguide material used in sensors, surface acoustic devices, transparent electrodes, and solar cells. Due to its excellent transparency and electron mobility, zinc oxide (ZnO) is the material with the best prospects for solar cells. An improved efficiency of 9.3% is seen for ZnO nanorods produced at 700.C and 5T deposition pressure. In applications requiring gas deterction, tin oxide (SnO2) is widely employed. Matal oxides (ZnO and SnO2) and polypyrrole (PPy) nanocomposites have an edge over other materials for developing sensing devices. The construction of sensing devices requires knowledge of the parameters of these nanocomposite thin films. Different technologies, including conductometric and optical sensors, are available for detection of hazardous and toxic gases. The surface plasmon resonance (SPR) technique is one of the oldest techniques for its application in gas sensing and researchers have exploited it for gas sensing applications. The SPR technique is an extremely sensitive technique which can be used for sensing minute changes near the boundary interface of the dielectric with the metal. The dielectric properties of any material can be studied by analysing the refractive index dispersion of its structure under the influence of an electromagnetic field. The sellmeier behaviour followed by the refractive index and dielectric dispersion with incident wavelength or photon energy. By matching the exceptionally low quantities (5ppm). This could enable the development of a sensor for detection of NH3 gas. The ZnO and polypyrrole composite thin film has been prepared for the detection of NH3 gas. A surface plasmon resonance gas sensor system composed of prism/Au/ZnO/PPy has been made utilising the optimal thickness of ZnO and PPy. To successfully exploited using the sensitive sensing interface of SnO2 and PPy. The SPR sensor exhibits a quick response time (Is) and high sensitivity (4.5x10-3 RIU/ppm) towards NH3 gas across a wide variety of concentrations (1 to 10ppm). Additionally, the dynamic behaviour was seen and the calibration curve's estimated sensitivity of 0.202/ppm would be used. The sensor was also tested for conductometric sensing.

Contents

1. Sensors and their applications. 2. Synthesis and characterization techniques. 3. Synthesis characterization, optimization, and gas sensing through ZnO/ polypyrrole nanocomposite. 4. Synthesis, characterization, optimization and gas sensing through SnO2/ polypyrrole nanocomposite. 5. Bibliography.

03. GARA (Neha)

Modeling and Simulation of Multigate Junctionless Transistors for low Power VLSI Design.

Supervisor: Dr. Sneha Kabra

Th 26641

Abstract

The demand for low power portable compact highspeed electronic gadgets such as personal digital assistants, cellular phones, laptops, computers etc. has propelled research and development of advanced low power semiconductor devices. The highspeed compactness portability and enhanced functionality in the design are essential requirements for low power systems. Thus, a suitable design approach that can lower the system's power requirements is the need of hour. In order to reduce the power, it is important to know the power distribution within the processor. Low power methodologies should be followed throughout the design process from system

level to process level in order to minimize the power dissipation of digital systems without compromising the overall performance of the circuit.to minimize the power dissipation of digital systems without compromising the overall performance of the circuit. Complementary metal oxide semiconductor (CMOS) technology is most widely used in integrated circuit design because it is easy to implement on silicon, has lower production cost and consumes least amount of power as compared to other logic families. In order to design digital circuits that consume less power device dimensions need to be reduced to sub-nanometre scales. But reduction of device size is constrained by various short channel effects. Multiple-gate field effect transistors have emerged as an alternative to planar devices due to the strong electrostatic control of gate over the channel. However multi gate architectures have technological problems because of the need for extremely steep doping profiles for sub 100 nm channel lengths. This problem has been resolved with the invention of junctionless transistor (JLT) in 2010. It lacks p-n junctions in the source channel drain path and consists of uniform doping throughout the device. A JLT requires high concentration of doping (1019 cm3) in the channel region to obtain a high drive current and reduce various short channel effects. Therefore in this dissertation the concept of multi gate FETs and junctionless FET is combined together to implement digital circuits for low power applications. In this work the low power design methodology is adopted at the device/process and logic/circuit level to implement various logic gates and combinational circuits. Interface trap charges (ITC) induced in the device due to hot carrier effect or damage due to process stress and radiation pose significant threat to reliability of short channel devices. Interface traps at Si-SiO2 interface are always present in a practical device and can cause degradation in various electrical characteristics threshold voltage drain current transconductance etc. Presence of traps shift the bias point of the device which is a big risk for circuit applications. Therefore, this thesis also coves the reliability analysis of JLT based logic gates and digital circuits in the presence of interface trap charges.

Contents

1. Introduction 2. Estimation of performance of double gate junctionless transistor in the presence of interface trap charges for digital applications. 3. Gate stack junctionless double gate transistor based 6t sram and study of the impact of interface trap charges on stability parameters. 4.Dielectric separated independent gates junctionless transistor based highly scaled digital logic circuits. 5. Investigation of reliability of junctionless finfet in the presence of interfacial defects, high temperature, and radiation. 6. Conclusions and future scope.

04. GUPTA (Shubhra)

Analytical Simulation of ZrS2Based Heterostructures for thin Film Solar Cells. Supervisor: Prof. P.K. Shishodia

Th 226636

Abstract

Recently, ongoing research in the field of optoelectronics has added transition metal chalcogenides (TMCs) to the list of upcoming technologies for numerous applications. This class of material possesses exceptionally interesting structural, chemical, optical and electrical properties. The rising interest of researchers in TMCs such as ZrS2, MoS2, WS2, ZrSe2, MoSe2, WSe2, MoTe2, WTe2 etc. has led to a large number of investigations for their prospective applications in field effect devices, photovoltaics, photodetectors, energy storage batteries, catalysts etc. This corresponds due to their peculiar band structures, nontoxic nature, ease of availability, high carrier mobility and thermal and chemically stable

nature. Amongst all the TMCs, zirconium disulphide(ZrS2) compound has been found to be a promising candidate for optoelectronic applications. High Hall Effect mobility of 1247cm2V -1 sec-1, good ntype conductivity and room temperature band gap of 1.7eV makes it unique for electronic and optoelectronic applications and can be considered as a potential semiconductor material for thin film solar cells. The aim of this work is to explore ZrS2 as a new solar cell material. The emphasis has been laid on numerical simulation of ZrS2 based solar cell on Solar Cell Capacitance Simulator(SCAPS). ZrS2 thin film junction formed with different absorber materials like Copper zinc tin sulphide(CZTS), Copper indium sulphide(CIS), Copper indium selenide(CISe) and Cadmium telluride(CdTe) has been optimized and compared. This study is based on minimizing the use of toxic buffer material by non-toxic and low-cost novel ZrS2 material in photovoltaic devices. Numerical efficiency of 9.72% has been reported for ZrS2/CZTS device and found to be the best amongst all the compared devices. Other performance parameters obtained are 25.16mA/cm2 (short circuit current density), 0.61V(open circuit voltage) and 68.86%(fill factor). External quantum efficiency(EQE) response has also been studied and the absorption of photons in visible range of spectrum has been observed in all the structures. The impact of buffer and absorber layer thickness, operating temperature, illumination intensity, series and shunt resistances on cell performance have been discussed in detail. (iv) These remarkable results obtained on simulating CZTS based solar cell with novel buffer layer material(ZrS2) has made it interesting to investigate for further improvement of cell parameters. Selenization of CZTS film has illustrated that it can be beneficial for efficiency enhancement. Electrical characteristics and spectral response of optimized ZrS2/CZTSSe heterostructure have been discussed. The obtained results have been compared with ZrS2/CZTS and ZrS2/CZTSe structures. Optimization of ZrS2/CZTSSe heterostructure has been illustrated by varying the selenium concentration using exponential grading law in SCAPS. At 0.44 content ratio of S/(S+Se) maximum efficiency of 16.50% has been obtained. Other performance parameters such as short circuit current density(Jsc), open circuit voltage(Voc) and fill factor(FF) interpreted at this ratio are 35.54mA/cm2, 0.6342V and 73.23% respectively. The influence of different device and geometric parameters such as thickness, doping, electron affinity and permittivity on solar cell performance has also been studied in detail. ZrS2/CZTS device performance has also been benefited by two terminal tandem configuration formed with MoS2/Si cell. ZrS2/CZTS/MoS2/Si tandem cell has been designed using wider bandgap ZrS2(1.7eV) based top cell and lower bandgap MoS2(1.2eV) based bottom cell. Initially, top and bottom cells have been optimized to obtain maximum efficiency under standalone conditions illuminated with AM1.5 spectrum. To obtain the cumulative tandem cell photovoltaic response, top and bottom subcells have been calibrated by varying ZrS2(0.05-2.0μm) and MoS2(0.1- 1.0μm) thicknesses. Short circuit current density in both the cells has been matched for ZrS2 thickness at $0.267\mu m$ and MoS2 thickness at $0.2\mu m$ for the Jsc value of 18.12mA/cm2 . Under optimized current matching conditions, top cell fed with AM1.5 spectrum presented an efficiency of 7.43% and bottom cell fed with filtered spectrum presented an efficiency of 8.44%. Overall solar cell parameters for ZrS2/CZTS/MoS2/Si tandem cell obtained are 12.54%(η), 18.12mA/cm2 (Jsc), 0.9966V(Voc) and 69.43%(FF).

Contents

1. Introduction and literature review. 2. Theoretical methods 3. Simulated analysis of ZrS2 as buffer layer with different absorber layer materials. 4. Computation of solar cell parameters for ZrS2/Cu2ZnSn-x)4 heterostructure. 5. Numerical analysis

of transition metal chalcogenide based tandem solar cell parameters. 6. Conclusion and Future Aspects.

05. KATIYAR (Suleshma)

Modeling and Simulation of Ambipolar Transport in Organic Field-Effect Transistor for Light Emitting.

Supervisor: Prof. Jyotika Jogi

Th 26639

Abstract

During the past 50 years, inorganic semiconductors such as silicon, gallium nitride and gallium arsenide have been the backbone of electronics industry. Progress in technology complementing silicon based electronics has led to advances in organic electronics, a field based on novel class of organic semiconductors (OSCs). With the discovery of conducting polymer, named polyacetylene or polythyne in 1977, huge research efforts have been put to study conjugated organic materials. Polyacetylene was found to exhibit high conductivity on doping and this opened up the entire new area of research in organic semiconductors. Organic semiconductor technology promised multitude of advantages such as low cost, low temperature processing, large area application and use of mechanically flexible and inexpensive substrates. Initially, the stability and performance of available organic semiconductors were found to be poor. However, with the continuous improvements in the processing and synthesis of new classes of molecular semiconductor materials, for example polythiophene, the prospects of using organic semiconductors commercially for devices such as Organic Light-Emitting Diodes (OLEDs), Organic Photovoltaic devices and Organic FieldEffect Transistors (OFETs) have increased. Though the performance of some organic semiconductor devices is lagging behind their inorganic counterparts, still some of these devices are already being supported by the market. For instance, Philips in 2002 introduced Sensotec Philishave, as the first product which used polymer LED technology based display. Following this, Kodak and Sony introduced OLED display based digital zoom camera and 27 inch OLED TV respectively. There has been no turning back since then and OLED technology displays, based on polyLEDs, have turned out to be ideal next generation displays. OLED technology has the advantage of being simple, and low cost as it requires fewer materials and manufacturing steps. Abstract Suleshma Katiyar ii Also, complete display can be manufactured on single piece of plastic or glass. Further, this technology offers wide viewing angle with better contrast and brightness. Transistors, which are key constituents of digital revolution, have been the most important electronic device for more than half a century now. In recent years, performance of silicon based transistors has seen remarkable advances with miniaturization, material processing and design. These advances in silicon technology are however achieved at increasing manufacturing cost, which forbids them for use in low cost applications. Further, the single crystalline silicon is available in the form of brittle and rigid wafers with a diameter of about 20-30 cm. This again imposes limitation of using silicon transistors over large areas, flexible surfaces and transparent substrates such as glass. Thin film transistors (TFTs), unlike silicon transistors can be practically fabricated on any substrates by subsequently depositing semiconductor material in the form of thin polycrystalline or amorphous films. TFTs also called thin film field-effect transistors, work on the same mechanism of modulating current. TFTs were first demonstrated in 1962 by Weimer. However, it was only in 1980's that the advances in device physics, material preparation and film deposition paved the way to commercially feasible TFTs. The electric current in a TFT flows in close vicinity to the semiconductordielectric interface. Hence, the properties of both the semiconductor and dielectric are crucial in determining TFT's electrical performance. Hydrogenated amorphous silicon (a-Si:H) is one of the most commonly used material for TFTs and was first demonstrated in 1979. However, a-Si:H lacks long range order and hence affects the electrical performance parameter, such as mobility of charge carriers, which is limited by collisions with ionized impurities, defects and thermal vibrations of lattice atoms. The electron mobility in a-Si:H TFT is 1 cm2 /Vs, which is about three orders lower Abstract Suleshma Katiyar iii than in the single crystalline silicon FET. Although the carrier mobility is lower, it is sufficient for applications such as active matrix liquid crystal displays (AMLCDs) where currents of the order of micro amps and switching speed up to few megahertz are required. The maximum process temperature required to fabricate a-Si:H TFT is 300°C, which is much lower than 1000°C, required to fabricate crystalline silicon FETs. This allows the use of inexpensive substrates, such as glass. Though the investment required for a-Si:H TFT is lower than crystalline silicon FET, it is still high for ultra-low cost applications. Further, the process temperature of 300°C does not allow for the use of more flexible and light weight polymeric substrates. Polymeric substrate often degrades when subjected to temperatures above 100-200°C. This is when the idea of using organic material as active semiconducting layer came into play, since the temperature processing of organic materials is compatible with polymeric substrates. The field-effect phenomenon in an organic material was first observed by Ebisawa et al. in 1983. They fabricated the transistor with polyacetylene as the active layer and using glass as the substrate material. The current modulation was however small due to large defect density and impurity, it demonstrated that the conductivity in polymers can be modulated by electric field. The first organic thin film or field-effect transistor (OTFT or OFET) with high current modulation was demonstrated by Tsumura et al. in 1986. They used low impurity density polythiophene thin film and fabricated the transistor on heavily doped silicon substrate. The early development of OFETs was mainly based on polymeric organic semiconductors. Small molecule organic semiconductor based OFETs are an alternative to polymer OFETs and are deposited by thermal evaporation in vacuum. Abstract Suleshma Katiyar iv The work carried out in this thesis provides analytical as well as empirical insights into the charge transport mechanism of OFET. Emphasis has been laid down on the ambipolar transport in the OFET, wherein both electron and holes contribute to current conduction. Ambipolar OFETs are necessary for applications such as complementary metal oxide semiconductor (CMOS) inverter. CMOS inverters, which consists of one n-type and one p-type transistors offer better noise margins and reduces power consumption. As ambipolar OFETs can transport both electrons and holes, they can be operated as n-channel or p-channel OFETs respectively, when subjected to appropriate bias conditions. Further, ambipolar OFETs can be operated in both negative and positive bias voltages. Thus, unlike CMOS inverters which when fabricated using unipolar OFETs, require two individual materials to act as pchannel or n-channel, ambipolar OFETs do not require micro-patterning of two individual channel material. In this way fabrication cost is reduced substantially. Ambipolar OFETs can also function as a more integrated light emitting device, commonly known as organic light-emitting transistor. Light emission takes place in the channel region when a suitable light-emitting organic semiconductor is used as active channel material. In the work presented in the thesis, position of light emission, which is the point of recombination of holes and electrons in the channel region is obtained, both as a function of gate source and drain source voltages. Numerical simulations have also been performed to study the light-emitting behavior in both unipolar and ambipolar OFETs. As traps or defect states, are inherent to organic or amorphous semiconductor, its influence during the formulation of a physics based model for ambipolar OFET has been considered in depth. In OFET, transport occurs by accumulation of charge carriers at the interface of organic semiconductor and dielectric interface. Hence, the Abstract Suleshma Katiyar v

influence of interface traps is crucial, and is therefore considered in the presented work. In Chapter 1, a detailed introduction about organic semiconductor and devices based on it is given. In addition to describing the fundamental properties of organic semiconductor, this chapter gives a glimpse of charge transport mechanism pertaining in organic semiconductor. Its differences with inorganic semiconductors are covered in brief. Importance has been given to ambipolar transport, since it is the motivation behind the research work and targets applications such as inverter circuits and light emission. In Chapter 2, numerical simulation of organic lightemitting transistors (OLETs) is presented. It describes unipolar and ambipolar OLET based on structure, materials and electrode specifications. Three different structures, based on light-emitting tris-(8- hhydroxyquinolinato) aluminum (alq3) and field effect material Pentacene (C22H14) are considered in this work. In Chapter 3, comprehensive modeling of ambipolar OFET is presented. Its considers electron accumulation mode, i.e., positive gate source and drain source voltages. Driftdiffusion approach has been used to calculate charge carrier density in the channel. Further, the model assumes constant mobility and applies classical physics to derive current-voltage relations in both unipolar and ambipolar regime. Various characteristics are evaluated as a function of bias voltages in both the regimes. The model has been derived for both above and sub threshold operation. In the subthreshold operation, it considers the effect of interface traps. In Chapter 4, empirical charge transport modeling of ambipolar OFET is performed while considering traps inside organic semiconductor. Charge transport models Abstract Suleshma Katiyar vi related to traps, such as multiple trap and release (MTR) theory and variable range hopping (VRH) theory are described. According to these models, conclusions drawn suggest that the traps lead to mobility becoming temperature and gate bias dependent. This fact is used empirically to derive current-voltage relation in ambipolar OFET in both above and subthreshold region. In Chapter 5, physics based model for ambipolar OFET is presented while considering trap limited conduction. Sources of traps are discussed in this chapter and multiple trap and release theory is utilized to formulate the model. For the above threshold operation tail traps in the organic semiconductor are considered. While for subthreshold and deep subthreshold operation deep trap states in the bulk of organic semiconductor and interface trap states are accounted for. In Chapter 6, conclusions drawn from the work are presented and also highlight the future scope of the work.

Contents

1. Introduction 2. Simulation of Alq3/pentacene OLETs based on various device architectures. 3. Modeling ambipolar charge transport in an organic field effect transistor. 4. Field-dependent mobility based empirical model for ambipolar OFETs. 5. Investigation and modeling of trap states in ambipolar OFET. 6. Conclusions and Future Scope of Work.

06. KASHYAP (Jyoti)

Study and Analysis of Absorption Enhancement by Surface Texturzation in Solar Cell Structure.

Supervisor: Prof. Udaibir Singh

Th 26642

Abstract

Photovoltaic checks all the marks when it comes to satisfy world's demand for environment friendly alternative energy source. In particular silicon solar cell offer enormous potential. Because of their abundance and technological maturity silicon solar cells are still the preferred PV technology over all others. However, silicon tends

to have very high surface reflectance approximately 30-40% of incident light is reflected from the bare silicon surface. Creating surface textures is one of the effective methods to significantly reduce front surface reflectance. The aim of this study was to investigate effect of surface texture on silicon solar cells. To achieve the above set goals, experimental studies are performed. A brief literature review revealed that texturization techniques use various etching approaches. The selection of etching technique and its results strongly depend on the choice of silicon substrate whether it is monocrystalline or multicrystalline. In this work alkaline anisotropic etching has been used to create pyramidal structures on the surface of a (100) oriented monocrystalline silicon solar cell. Alkaline etching is anisotropic in nature which means that it occurs more readily in one crystallographic orientation of silicon than another. As a result the textured surfaces are composed of slow etching palnes in the end. When (1000 oriented planes are exposed to such etching techniques intersections of (111) facets are revealed resulting in a pyramidal morphology. The pyramids created with the optimal etching time and other procedure parameters all have a high facet till angle 54.74 which guarantees improved front surface antireflection properties as well as uniform surface coverage.

Contents

1. Introduction. 2. Experimental and characterization technique. 3. Surface texturization for reduction of light reflection in ZnO/Si heterojunction. 4. Electrical characterization of n-ZnO/p-Si heterojunction prepared with textured silicon substrate. 5. Improved photovoltaic performance of heterojunction solar cell by the incorporation of highly conducting rGO into ZnO nanocomposite on textured si substrate. 6. Conclusions and future scope of work.

07. NATH (Jyoti Prasad)

Evanescent Coupling Based Multiplexers for Multi-Channel Guided wave Optical Interconnects.

Supervisor: Dr. Geetika Jain Saxena

Th 26637

Abstract

With the advancement of technology, the size of the transistors is reducing and has reached its physical barrier. Hence, technology is currently heading towards multicore and many-core processors on a single chip with an extensive electrical onchip interconnect network. The existing copper wires suffer from a huge ohmic loss at the high frequencies due to the skin effect. The electrical power consumed in the interconnect network is expected to reach to ~80% of the total microprocessor power. Optical interconnects that offer higher bandwidth scalability and low power consumption are emerging as a promising approach toward replacing the conventional copper-based electrical interconnects for on-chip, chip-to-chip and board-to-board interconnects. CMOS fabrication compatibility has made possible the co-existence of silicon photonic circuits with the existing electronics on the same silicon substrate. Hence, the integration of Silicon-on-Insulator (SOI) waveguides as optical interconnects with electronic processors provides a perceptible solution to replace the electrical interconnects. The high refractive index contrast between silicon and silicon oxide has enabled the miniaturization of the photonic waveguides to nanometer dimensions. Mode Division Multiplexing (MDM) in which each individual guided mode of a multimode waveguide carries a different data channel at a single wavelength, has gained attention towards increasing the bandwidth of SOI based optical interconnects. Multiplexers and De-multiplexers are required to couple/decouple individual data channels to/from different modes of the shared multimode bus waveguide for multichannel operation. This thesis is focused on the design of multiplexers and demultiplexers based on the use of mode selective evanescent coupling between closely placed silicon waveguides. We start with introducing electromagnetic modes and their propagation in silicon-oninsulator (SOI) strip waveguides with two-dimensional confinement. The guided fields of these dielectric waveguides have a decaying evanescent field outside of the waveguide core. Hence, when two waveguides are placed in close proximity, their evanescent fields interact to form a coupled waveguide configuration in which power exchange is possible between the waveguides. The Coupled Mode Theory (CMT) has been an alternate intuitive analytical mathematical tool for analysis of the coupled Abstract ii waveguide configurations. We present the coupled mode analysis for a coupled configuration of a single mode and a multimode waveguide to show that it is possible to couple from single mode waveguides to the specific mode of a multimode interconnect waveguide. All the multiplexers for mode division multiplexing designed in this thesis are based on this concept. In our design of multiplexers, we have introduced a novel concept of coupling two input modes simultaneously using two collaterally arranged input waveguides. We used this concept to design compact mode multiplexers and de-multiplexers. We first designed a three-channel mode division (de)multiplexer for (de)multiplexing three independent channels from three single mode waveguides into three modes of a 1 μ m wide multimode waveguide. A short coupling section of 24 µm is possible with collateral coupling instead of sequential coupling. We also extended the (de)multiplexer by adding another collocated coupler section with a wider bus waveguide of width 1.7 μ m sequentially. The 3-mode and 5-mode (de)multiplexers are obtained with low insertion loss and cross talk over the entire C-band. As the silicon waveguide supports two types of orthogonally polarized modes, TE mode and TM mode, the number of channels can be further increased by using both polarized modes. Hence, we extended the design concept of collocated couplers to design a sevenchannel hybrid mode- and polarization-division multiplexer by using collocated coupler sections, and a polarization beam splitter. The design is fabrication tolerant: for a waveguide width error of ±10 nm, the performance of the device in terms of insertion loss and crosstalk is obtained as <-21 dB, respectively. To achieve a further increase in the bandwidth, the mature wavelength division multiplexing technique can be used, employing different wavelength channels as individual information carriers. In recent years, various active and passive photonic devices have beendeveloped at 2 μm wavelength including switches, modulators, photodetectors, lasers, etc. We designed an 8-channel dual band mode (de)multiplexer by using three collocated directional coupler sections, which combine wavelength division multiplexing at 1.55 µm and 2 μm wavelength simultaneously with the multichannel mode division multiplexing. The multiplexer response has a broad bandwidth of >100 nm, and insertion loss and crosstalk for both the waveband is <- 27 dB, respectively.

Contents

1. Introduction 2. Dielectric optical waveguides. 3. Coupled mode analysis of evanescently coupled waveguides. 4. Compact mode division (de) multiplexer based on collaterally coupled SOI waveguides. 5. SOI based compact mode-and polarization division (de) multiplexer for on chip optical interconnects. 6. SOI based compact 8-channel wavelength and mode division (de) multiplexer for on chip optical interconnects. Scope for Future Work. Bibliography. Reprints of the publications.

08. PANDEY (Priyanka)

Modeling, Simulation of Insulator and Channel Engineered Polarity Controllable FETs for Sensing Applications.

Supervisor: Dr. Harsupreet Kaur

Th 26640

Abstract

With the continuous sealing of device dimensions the complementary metal oside semiconductor (CMOS) technology has evolved tremendously in terms of both high performance and compact circuit topologies. However with progressive device sealing the issues of increased parasitic source/drain (S/D) resistance degraded current drivability increased power dissipation along with reduced gate controllability have become prominent and these need to be addressed. In order to counter these issues schottky junctions based polarity controllable FETs (PC-FETs can appear as promising candidates because of their numerous advantages such as reduced parasitic resistance abrupt metal semiconductor junctions and low thermal processing. Further due to their unique property of dual programmable behaviour, PC-FETs exhibit effective reduction in transistor count which leads to improvement in chip density. However the other issues such as low current drivability and increased power dissipation are critical and need to be addressed. The afore mentioned issues such as reduced current drivability increased static power dissipation etc have led to the present work and the thesis discusses extensively about the polarity controllable FETs. Various promising alternatives including insulator and channel engineering are proposed and investigated exhaustively to overcome the drawbacks of PC-FETs and to improve device performance.

Contents

1. Introduction 2. Impact of insulator engineering on single gate polarity controllable FET. 3. Impact of insulator engineering on dual gate polarity controllable FET. 4. Impact of channel engineering on dual gate polarity controllable FET. 5. Polarity controllable FET as ph sensor. 6. Polarity controllable FET as gas sensor. 7. Conclusion and Future Scope. Bibliography, Publications.

09. RAKESH

Study of Metal/Semiconductor Clad Waveguides and Their Applications.

Supervisors: Prof. Geeta Bhatt

Th 26643

Abstract

The last few decades have witnessed much significant research in the field of semiconductor and metal-clad optical waveguides. On the basis of semiconductor or metal thin film cladding, electromagnetic resonance phenomenon such as surface plasmonic resonance (SPR) and Lossy Mode resonance (LMR) can be observed in various multilayer waveguide structures. In the case of SPR, coupling takes place between evanescent wave and surface plasmons, which leads to the phenomenon of surface plasmonic resonance. This phenomenon generally occurs in metal thin films, but at higher wavelengths metal oxides such as indium tin oxide (ITO), zinc oxide (ZnO) etc. also supports this kind of resonances. On the other hand, lossy mode resonance (LMR) can be observed when the coupling occurs between guided mode and the lossy modes supported by the semiconducting thin film. Recently various articles have been published based on lossy mode resonance supported by the Transparent Semiconducting Oxides (TSMO) thin films such as ITO, ZnO, SnO2.

This study is focused on the electromagnetic resonances supported by the Metal/ Semiconductor clad waveguides and their application of sensing. In last few decades many optics-based sensing techniques have also been established to be used in various applications related to gas sensing, chemical sensing, biosensing and magnetic field sensing etc. The sensing mechanism mainly depend on the characteristics of thin film deposited either on the waveguide or a prism which supports electromagnetic resonances. SPR based techniques and mechanisms have been ruled in the area of optical sensing, but unfortunately sensitivity limit for SPR sensors seems to have been attained. The susceptibility to oxidation of metal film and requirement of additional coating layers of dielectric or less reactive metals lead to reduce the sensitivity of SPR sensors. Also, to shift the operating point of SPR based sensor towards biosensing, it requires a high index cover layer which drastically reduces the sensitivity. Among the optical waveguide sensing techniques based on the concept of refractive index (RI) variation of analyte, the most recently proposed one is the LMR based sensing. Thin absorbing films with small imaginary and large real part of refractive index, support lossy mode resonances. Thus, in the present study prism coupled sensor structure with ZnO thin Film is presented for sucrose sensing and investigated using spectral and ii angular interrogations. An additional matching layer is also introduced between the prism and ZnO to provide better phase matching between the lossy modes and the guided modes to enhance the sensitivity of the sensor. The thicknesses of ZnO are optimized for obtaining sharp LMR reflectance curves using theoretical simulations. The best simulated sensing configurations are fabricated for both s- and ppolarizations of light to sense the change in sucrose concentration. Sucrose is an important analyte in clinical and industrial food analysers and that is why used as the sample analyte for sensing. Also, graphene coated optical fiber structure has been exploited theoretically for refractive index sensing within visible operating region. Here, a high refractive index polymer layer is used as the matching layer to generate lossy mode resonances in the desired spectrum. It is observed that multilayer graphene coating supports much sharper and narrower resonances than the graphene monolayer. Sensing characteristics with variation in number of graphene layers and polymer layer thickness are investigated with different polarizations of light. It is observed that polymer layer act as the catalyst in enabling the structure to support resonances and shifting the operating region in visible spectrum. It is believed that visible range operation of the proposed structure will make it cost effective and highly suitable for the development of bio-chemical sensors

Contents

1. Introduction 2. Sensor design based on electromagnetic resonances. 3. Generation of lossy mode resonances using ZnO thin film. 4. Fabrication of prism coupled sucrose sensor 5. Design of grapheme coated fiber optic sensor for visible range. 6. Conclusion and Future Scope.

10. SINGH (Preeti)

TCAD Based Investigation of Advanced High Electron Mobility Transistor (HEMT) Structures for High Power and High Frequency Applications.

Supervisor: Prof. Mridula Gupta

Th 27114

Abstract

Silicon has been the backbone of semiconductor technology for nearly six decades driven by moore's law. However. Silicon is approaching its theoretical limit with the growing demand for high operating voltage high output power and high frequencies for power electronics and RF applications. In recent years wide bandgap materials such as gallium nitride (GaN) have become a promising alternative for such applications owing to the wide bandgap higher breakdown strength hight carrier density and high operating temperature as compared to conventional silicon and GaAs material. GaN-based devices namely AIGaN/GaN high electron mobility Transistors (HEMTs) exhibit high efficiency low on resistance lower switching losses and high breakdown voltages. In addition high mobilities high electron saturation velocities low parasitic capacitances and reduced noise factor makes single gate (SG) AIGaN/GaN HEMTs suitable for RF applications. Nevertheless conventional schottky gated SG-HEMT devices exhibit significant gate leakage current which contributes to standby power dissipation and degrades RF performance. Therefore SG-HEMT with gate dielectric SG Metal insulator semiconductor HEMT (SG-MISHEMT) has been employed in this thesis work. Additionally higher Johnson's figure of merit simultaneous achievement of high breakdown voltage and high frequencies of operation is a critical challenge for SG-MISHEMTs. Further SG-MISHEMT performance is also restricted by several reliability issues such as the current collapse phenomenon source drain punch through charges at oxide barrier interface short channel effects. Therefore the work presented in this thesis addresses the challenges of dual gate (DG) AIGaN/GaN MISHEMT for high power switching and RF applications using modelling and TCAD simulations.

Contents

1. Introduction. 2. Performance assessment of dual gate AIGaN/GaN MISHEMT for DC and RF Applications. 3. Trade-off optimization of dual gate MISHEMT for high power applications. 4. Asymmetric dual gate- MISHEMT for law noise application. 5. Investigation of e-mode dual gate MISHEMT for high power switching application. 6. Conclusion and future scope.

11. SEHGAL (Himani Dua)

Modeling and Simulation of Junctionless FinFET for Sensing Applications.

Supervisor: Dr. Sneha Kabra

Th 27271

Abstract

In the last few decades the semiconductor industry has progressed tremendously in design and development of various sensors for applications in area of medical instrumentation gas detection agriculture management and food safety. In the recent times various FET architectures like MOSFETs GAA-JLT and nanowire FETs have been proposed as sensors to attain high sensitivity low response time and high selectivity. Early diagnosis of numerous life threatening disorders is crucial as it enables early intervention and treatment which lowers the death rate. The presence of different biomolecules in the human body are detected in order to diagnose these disorders. In addition to the identification of biomolecules the detection of toxic gases is also crucial. In order to prevent the harmful effects that various gases including hydrogen chloroform methane and iso-propanol have on the environment and living organisms portable sensors to detect these gases must be designed and developed on large scale. The investigation of how radiation affects various FET based memory devices used in satellite communication is another area that requires attention. Although there are several techniques available for designing of sensors but FET based sensors offer better characteristics in terms of excellent sensitivity high selectivity a rapid response time how operating voltages and low cost.

Contents

1. Introduction. 2. Modelling and simulation of junction less finFET for biosensing applications. 3.Detection of highly invasive breast cancer cells using FinFET device. 4. Modeling and simulation of juncitonless FinFET for detection of hydrogen gas sensor using catalytic metal gate. 5. Detection of poisonous gases using JL FinFET with conducting polymer gate. 6. Designing and reliability analysis of radiation hardened stacked gate junctionless FinFET and CMOS inverter . 7. Conclusions and future scope.

12. YADAV(Hina)

High gain micro strip antennas for power harvesting.

Supervisors: Prof. Mridula Gupta

Th 26638

Abstract

Over the last few decades there is an unprecedented increase in energy requirements witnessed around the globe. With this the quickly diminishing fossil fuel reserves suggest the urgent need for a secure long lasting alternative energy resource. The free available ambient microwave energy is one such alternative for low power devices. A major merit associated with RF energy is its very less dependency on the weather conditions and availability at all the time of the day. The power level is very high within 50cm radius from a cell tower. This can cause radiation health hazards such as muscle and joint pain tingling memory loss nausea dizziness and sometimes even leading to cancer prominently RF energy freely available in the vicinity of mobile towers gives and opportunity to se as a continuous source of renewable energy and helps reduce radiation hazards. Wireless networks are an omnipresent RF energy source therefore RF energy harvesting system to operate at 4G LTE networks over BAND 1 LTE FDD (2100 MHz) BAND 3 LTE FDD 91800 MHz) has been developed. It covers the lower and upper bounds of these two bands completely. AN energy harvester also known as rectenna consists of an antenna to receive RF waves followed by an impedance matching network and rectification circuit. Antenna is an important part in RF harvesting units for receiving maximum power. Microstrip antenna with differential configuration has recently emerged improving efficiency of overall harvesting unit. Important consideration while designing the antenna are impedance matching radiation pattern its size and the application for which the harvested energy will be used. This thesis investigates the possible application of high gain broadband microstrip antennas for RF power Harvesting. In order to do so different configurations of microstrip antennas have been investigated and new topologies have been introduced to achieve higher RF-DC conversion efficiency.

Contents

1. Introduction 2. Differential microstrip patch rectenna featuring consistent high gain over a wide operating bandwidth. 3. Differential multi-stacked microstrip antenna for wireless energy harvesting. 4. Broadband microstrip rectenna for wide impedance range. 5. Conclusion and Future Scope.